2D MATERIALS: PROSPECTS FOR ELECTRONICS

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# A Few US Programs on Nanoelectronics

- **Univ. Nebraska-Lincoln**
- **Univ. Wisconsin-Madison**
- **SUNY Buffalo**
- **UC-Irvine**
- **Univ. Oakland**
- **Univ. Delaware**

**SUNY-Albany**
- **Purdue**
- **U. Virginia**
- **Cornell**
- **GTR**
- **Columbia U**
- **Brown**

**UT-Austin**
- **UT-Dallas**
- **NCSU**
- **Texas A&M**
- **UCSD**
- **Harvard**

**MIT**
- **Notre Dame (2)**
- **Columbia / Florida**

**University of Minnesota**
- **Carnegie Mellon**
- **U. Wisconsin**
- **U. Nebraska**
- **U. Alabama**
- **Colorado**
- **U. Arizona**
- **State**
- **UC/ Berkeley**
- **Johns**
- **UC/ Riverside**
- **Hopkins**
- **UC/ Santa**
- **MIT**
- **Barbara**
- **Ohio State**
- **UT/ Austin**
- **Penn State**
- **U. Iowa**
- **Purdue**
- **U. Michigan**

**CALTECH**
- **UC/ Berkeley**
- **Columbia**
- **UC/ Irvine**
- **Cornell**
- **UC/ Riverside**
- **MIT**
- **UC/ Santa**
- **NC State**
- **Barbara**
- **Purdue**
- **U of PA**
- **Rice**
- **WVA**
- **Stanford**
- **Yale**

**Carnegie Mellon**
- **UT/Austin**
- **GA Tech**
- **UT/Dallas**
- **Penn State**
- **Purdue**
- **UC/ Berkeley**
- **UC/ San Diego**
- **UC/ Santa Barbara**

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**TEXAS INSTRUMENTS**

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**FAME**

**UCLA**

**Least Cost Energy Systems Technology**
NRI MISSION STATEMENT – 2006 TIMEFRAME

• **NRI MISSION**: Demonstrate novel computing devices capable of replacing the CMOS FET as a logic switch in the 2020 timeframe.

• These devices should *show significant advantage over ultimate FETs* in power, performance, density, and/or cost to enable the semiconductor industry to extend the historical cost and performance trends for information technology.
  – To meet these goals, NRI pursues five *research vectors*:
    • **NEW DEVICE**: Device with alternative state vector
    • **NEW WAYS TO CONNECT DEVICES**: Non-charge data transfer
    • **NEW METHODS FOR COMPUTATION**: Non-equilibrium systems
    • **NEW METHODS TO MANAGE HEAT**: Nanoscale phonon engineering
    • **NEW METHODS OF FABRICATION**: Directed self-assembly devices
  – Finally, it is desirable that these technologies be capable of integrating with CMOS, to allow exploitation of their potentially complementary functionality in heterogeneous systems and to enable a smooth transition to a new scaling path.
COMPUTATIONAL VARIABLES

• Charge: CMOS, TFET

• Electric Dipole: FeFET

• Magnetic Dipole: NML, SWD, and ASL

• Orbital State: BiSFET

• Strain: PiezoFET
FIRST PRINCIPLES PREDICTIONS OF 2D CRYSTAL BAND ALIGNMENTS

Calculated by density functional theory

### List of Devices Under Consideration

<table>
<thead>
<tr>
<th>Device Name</th>
<th>Acronym</th>
<th>Input(s)</th>
<th>Control</th>
<th>Int. State</th>
<th>Output</th>
<th>Material</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si MOSFET high perf.</td>
<td>CMOS HP</td>
<td>V</td>
<td>Vg</td>
<td>Q</td>
<td>V</td>
<td>silicon</td>
</tr>
<tr>
<td>Si MOSFET low voltage</td>
<td>CMOS LV</td>
<td>V</td>
<td>Vg</td>
<td>Q</td>
<td>V</td>
<td>InAs</td>
</tr>
<tr>
<td>van der Walls FET</td>
<td>vWFET</td>
<td>V</td>
<td>Vg</td>
<td>Q</td>
<td>V</td>
<td>MoS₂</td>
</tr>
<tr>
<td>Homojunction III-V TFET</td>
<td>HomTFET</td>
<td>V</td>
<td>Vg</td>
<td>R</td>
<td>V</td>
<td>InAs</td>
</tr>
<tr>
<td>Heterojunction III-V TFET</td>
<td>HetTFET</td>
<td>V</td>
<td>Vg</td>
<td>R</td>
<td>V</td>
<td>GaSb/InAs</td>
</tr>
<tr>
<td>Graphene nanoribbon TFET</td>
<td>grnTFET</td>
<td>V</td>
<td>Vg</td>
<td>R</td>
<td>V</td>
<td>graphene</td>
</tr>
<tr>
<td>Interlayer tunneling FET</td>
<td>ITFET</td>
<td>V</td>
<td>Vg</td>
<td>R</td>
<td>V</td>
<td>graphene</td>
</tr>
<tr>
<td>Two D Heterojunction Interlayer TFET</td>
<td>ThinFET</td>
<td>V</td>
<td>Vg</td>
<td>R</td>
<td>V</td>
<td>WTe₂/SnSe₂</td>
</tr>
<tr>
<td>GaN TFET</td>
<td>GaNFT</td>
<td>V</td>
<td>Vg</td>
<td>R</td>
<td>V</td>
<td>GaN</td>
</tr>
<tr>
<td>Transition Metal Dichalcogenide TFET</td>
<td>TMDTFET</td>
<td>V</td>
<td>Vg</td>
<td>R</td>
<td>V</td>
<td>WTe₂</td>
</tr>
<tr>
<td>Graphene pn-junction</td>
<td>GpnJ</td>
<td>V</td>
<td>Vg</td>
<td>R</td>
<td>V</td>
<td>graphene</td>
</tr>
<tr>
<td>Ferroelectric FET</td>
<td>FEFET</td>
<td>V</td>
<td>Vg</td>
<td>P</td>
<td>V</td>
<td>PZT</td>
</tr>
<tr>
<td>Negative capacitance FET</td>
<td>NCFET</td>
<td>V</td>
<td>Vg</td>
<td>P</td>
<td>V</td>
<td>PZT</td>
</tr>
<tr>
<td>Piezoelectric FET</td>
<td>PiezoFET</td>
<td>V</td>
<td>V</td>
<td>σ</td>
<td>V</td>
<td>AIN</td>
</tr>
<tr>
<td>Bilayer pseudospin FET</td>
<td>BisFET</td>
<td>V</td>
<td>Vg</td>
<td>B, C</td>
<td>V</td>
<td>graphene</td>
</tr>
<tr>
<td>Excitonic FET</td>
<td>ExFET</td>
<td>V</td>
<td>Vg</td>
<td>B, C</td>
<td>V</td>
<td>MoS₂/MoSe₂</td>
</tr>
<tr>
<td>Metal-insulator transistor</td>
<td>MITFET</td>
<td>V</td>
<td>Vg</td>
<td>Orb</td>
<td>V</td>
<td>NdNiO₃</td>
</tr>
<tr>
<td>SpinFET (Sugahara-Tanaka)</td>
<td>SpinFET</td>
<td>V</td>
<td>Vg, Vm</td>
<td>Q, M</td>
<td>V</td>
<td>CoFeB</td>
</tr>
<tr>
<td>All-spin logic</td>
<td>ASL</td>
<td>M</td>
<td>V</td>
<td>M</td>
<td>M</td>
<td>CoPtCrB</td>
</tr>
<tr>
<td>Charge-spin logic</td>
<td>CSL</td>
<td>I</td>
<td>V</td>
<td>M</td>
<td>I</td>
<td>CoPtCrB</td>
</tr>
<tr>
<td>Spin torque domain wall</td>
<td>STT/DW</td>
<td>I</td>
<td>V</td>
<td>M</td>
<td>I</td>
<td>CoFeB</td>
</tr>
<tr>
<td>Spin majority gate</td>
<td>SMG</td>
<td>M</td>
<td>V</td>
<td>M</td>
<td>M</td>
<td>PMN-PT</td>
</tr>
<tr>
<td>Spin torque oscillator</td>
<td>STO</td>
<td>I</td>
<td>V</td>
<td>M</td>
<td>I</td>
<td>CoPtCrB</td>
</tr>
<tr>
<td>Spin wave device</td>
<td>SWD</td>
<td>M</td>
<td>I or V</td>
<td>M</td>
<td>M</td>
<td>PMN-PT</td>
</tr>
<tr>
<td>Nanomagnetic logic</td>
<td>NML</td>
<td>M</td>
<td>B or V</td>
<td>M</td>
<td>M</td>
<td>PMN-PT</td>
</tr>
</tbody>
</table>
SWITCHING ENERGY VS. DELAY OF A 32-BIT ADDER

Benchmarking emerging devices vs. CMOS

Are TFET the solution?

Transfer characteristics ($I_{DS}$ versus $V_{GS}$)

Log $I_{DS}$

$I_{on}$ $V_{DS} = V'_{DD}$ $V_{DD}$

$I_{off}$ $V'_{DD}$

$SS = \frac{dV_{GS}}{d \log(I_{DS})}$

Need a $SS << 60 \text{ mV/dec}$

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DOUBLE BILAYER ITFET: FABRICATION AND ROTATIONAL ALIGNMENT

- Straight edges assumed to be principal crystal axes
- Layer transfer done while keeping track of orientation

DOUBLE BILAYER ITFET: INTERLAYER I-V CHARACTERISTICS AT RT

Vertical tunneling field-effect transistor using a stacked double bilayer graphene (BLG) and hexagonal boron nitride heterostructure

6 monolayers thick BN NDR!

5 monolayer thick BN NDR!

S. Kang et al. IEEE ELECTRON DEVICE LETTERS, VOL. 36, NO. 4, APRIL 2015
2D-2D Tunneling in Heterojunction TFETs

Gate controlled band-to-band tunneling and NDR!

• "If you cannot measure, your knowledge is meager and unsatisfactory." Lord Kelvin

and …….

• “there cannot be devices without materials”

and

mining is NOT an option as a source of compounds/ML for the SC industry …..
GRAPHENE SINGLE CRYSTALS: FROM MICRONS TO CENTIMETER

2005
Monolayer graphite

Novoselov et al., PNAS 2005

2013-15
Single Crystal Graphene and BLG

Hao et al., Science 2013
Hao et al., submitted for pub
MOBILITY OF GRAPHENE AND MoS$_2$ AND PREPARATION METHODS

HEXAGONAL BORON NITRIDE

Bulk h-BN

CVD h-BN/m Metals

Large single crystal controlled thin films needed

A. Ismach et al., ms in preparation
S. Sonde et al., ms in preparation

Unit cell = (2.5 ± 0.4) Å
RMS roughness = (0.35 ± 0.10) Å

A. Ismach et al., ms in preparation
S. Sonde et al., ms in preparation
**TMDs**

**Bulk Crystal of MoS$_2$**

**TMD Heterostructures by CVD**

- Vertical WS$_2$/MoS$_2$ bilayer
- In-plane WS$_2$/MoS$_2$ monolayer

**TMD Heterostructures By MBE**

MoS$_2$ HfSe$_2$

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http://www.hggraphene.com/PeriodicTableElements/Mo.php
Yongji Gong, Nature Mat., V. 13, 2014
DIFFERENTIAL CONDUCTANCE AT ROOM TEMPERATURE ON NATURAL MoS$_2$

Electrical properties variations across MoS$_2$ can be correlated with local variations in stoichiometry as well as metallic and structural defects.

R. Addou et al., ACS Appl. Mater. Interfaces, 2015, 7 (22), pp 11921–11929
2D MATERIALS GROWTH SIMULATIONS

- 2H structure (L), 1T structure (R)

- Inhomogeneous adsorption energy: -0.65 eV
- Homogeneous adsorption energy: -2.56 eV
- Each bond: 2 eV
- Deposition rate: 0.1 ML/s
- 1E13 vibrations per second

- In 2H structure, the second triangle is upside-down, in 1T they are pointing at the same direction.
FROM A FEW MM TO 300-450 MM IN DIA
AND MANY KM/MONTH IN TOTAL LENGTH

1949-50
G. Teal, IEEE TED, ED-23 (7) 1976

Today

http://www.crystal-material.com/Single-Crystal-Materials/Silicon-Si-single-crystal.html
http://pcplus.techradar.com/2009/05/21/how-silicon-chips-are-made/
SUMMARY

• New devices will need rotationally aligned layers and will drive the need (similar to lattice matching for cubic system):
  – To grow single crystals
  – Selective single crystal growth … heteroepitaxy

• Defect control ("bulk" and surface)
  – Chalcogenide materials are especially sensitive to the creation/formation of point defects (vacancies) – bulk and surface

• Need to determine fundamental properties of materials and a deeper understanding of the materials growth processes
  – Metrology
  – Standards

• How about scaled 2D-materials-based devices … submicron???