DARPA/SRC STARnet

Avram Bar-Cohen
Program Manager
MTO

US-EU Workshop on 2D Layered Materials and Devices

April 23, 2015
STARnet Funded Universities

University of Minnesota

UC/Irvine
UC/Riverside
UC/Santa Barbara
U. Iowa
U. Michigan
U. Nebraska
U. North Texas
U. Arizona

University of Michigan

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Duke
GA Tech
Harvard
MIT
Northeastern
Princeton
Stanford
UC/Berkeley
UCLA
UC/San Diego
UIUC
UVA
U. Washington

Notre Dame

CALTECH
Carnegie Mellon
U. Michigan
UT/Dallas
U. Washington

UIUC

Carnegie Mellon
Princeton
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UC/Berkeley

UC/Berkeley

UCLA

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UT/Austin

U. Iowa

42 Universities in 24 States Distribution Statement "A" (Approved for Public Release, Distribution Unlimited)
STARnet Centers

Materials/Devices Centers

Function Accelerated nanoMaterial Engineering (FAME)
Jane P-C Chang, UCLA

Theme 1: Multiferroics and Multifunctional Materials
- Perpendicular Magnetic Materials (Chung-Ah Oh)
- Spintronic Interface Engineering (Hong-IN Ahn)
- Spin Channel Materials (Chun-Geun Jo)

Theme 2: Multimetal/Spintronic Materials
- Materials for Nanoelectronics (Rakesh Dhawan)
- Role of Materials in Spintronics (Philipp Gegen

Theme 3: Van der Waals Materials (Philip Cvejanovic)
- Physical, Mechanisms & Device Prototyping (Rogelio Laskowski)

Theme 4: Physics, Mechanisms & Device Prototyping
- Spintronic Interfaces (Nikolai Bogdanov)
- Spin Transport and Interfaces (Hong-IN Ahn)
- Spin Transport and Magnetization Dynamics (Philipp Gegen

Center Focus:
- Quantum nanostructures for enabling analog, logic and memory devices and beyond Boolean computation

Center for Spintronic Materials, Interfaces and Novel Architectures, J-P Wang, UM

Center for Low Energy Systems Technology
Alan Seabuagh, Notre Dame

Center Focus:
- Exploration of solid state phenomena to extend device performance to achieve fundamental limits of ultra low voltage and power

2D Material Research across Materials/Devices Centers

TerraSwarm (TSRC-Internet of Things), Edward A. Lee, UC Berkeley

Center Focus:
- Pervasive integration of smart, networked sensors and actuators into our connected world through an open and universal systems architecture

The Center for Future Architectures Research
Todd Austin, UMi

Center Focus:
- Application driven architectures leveraging emerging circuit fabrics, such as 3D interconnect, novel memories and programmable logic

Systems on Nanoscale Information fabrics
Naresh Shanbhag, UIUC

Center Focus:
- Design of intelligent embedded systems on nanoscale CMOS and beyond CMOS device fabrics.

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Center Focus:
• Quantum nanostructures for enabling analog, logic and memory devices and for beyond Boolean computation.
Center for Spintronic Materials, Interfaces and Novel Architectures, J-P Wang, U. Minnesota

Center Focus:
• Spin-based memory and computation with magnetic materials, spin transport, novel spin-transport materials, spintronic devices, and circuits

C-SPIN Jian-Ping Wang, Director
The Center for Spintronic Materials, Interfaces and Novel Architectures (C-SPIN) seeks to overcome barriers to realizing practical spin-based memory and logic technology by assembling experts in magnetic materials, spin transport, novel spin-transport materials, spintronic devices, circuits, and novel architectures.
Center for **Low Energy** Systems Technology  
Alan Seabaugh, U. Notre Dame

Center Focus:  
• Exploration of solid state phenomena to extend device performance to achieve fundamental limits of ultra low voltage and power

**LEAST** Alan Seabaugh, Director  
The Center for Low Energy Systems Technology (LEAST) explores the physics of new materials and devices to enable more energy-efficient integrated circuits and systems.
DARPA MTO invested in graphene in 2007...

Graphene Review: An Emerging RF Technology

<table>
<thead>
<tr>
<th>Metric</th>
<th>Unit</th>
<th>Phase I</th>
<th>Phase II</th>
<th>Phase III</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>GNG Metrics</strong></td>
<td></td>
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<tr>
<td>Graphene Active Area</td>
<td>mm²</td>
<td>50 x 50</td>
<td>Wafer diam. ≥ 100 mm</td>
<td>Wafer diam. ≥ 200 mm</td>
</tr>
<tr>
<td>Uniformity</td>
<td>N</td>
<td>N ≥ 0 (1)</td>
<td>N ≥ 0 (2)</td>
<td>N ≥ 0 (3)</td>
</tr>
<tr>
<td>Carrier Hall Mobility</td>
<td>cm²/Vs</td>
<td>≥ 10,000</td>
<td>≥ 15,000</td>
<td>≥ 15,000</td>
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<tr>
<td>Carrier FET Mobility</td>
<td>cm²/Vs</td>
<td>≥ 5,000</td>
<td>≥ 10,000</td>
<td>≥ 15,000</td>
</tr>
<tr>
<td>$V_{th}$ (device bias)</td>
<td>V</td>
<td>1.0</td>
<td>0.5</td>
<td>0.25</td>
</tr>
<tr>
<td>$I_{on}$ (2)</td>
<td>μA/μm</td>
<td>≥ 250</td>
<td>≥ 1000</td>
<td>≥ 2000</td>
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<tr>
<td>$I_{off}$ (2)</td>
<td>μA/μm</td>
<td>1</td>
<td>100</td>
<td>1000</td>
</tr>
<tr>
<td>$f_{max}$ (1)</td>
<td>GHz</td>
<td>&gt; 300</td>
<td>&gt; 300</td>
<td>&gt; 500</td>
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<tr>
<td>$f_{max}$ (1)</td>
<td>GHz</td>
<td>&gt; 300</td>
<td>&gt; 300</td>
<td>&gt; 500</td>
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<tr>
<td>Demonstration Circuit</td>
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<tr>
<td>W-band LNA</td>
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<tr>
<td>Frequency: 50 GHz</td>
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<tr>
<td>Gain: ≥ 15 dB</td>
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<tr>
<td>Noise Figure: ≤ 1 dB</td>
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<tr>
<td>Cross wafer yield: ≥ 90%</td>
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</table>

(1) Control number of electrically active layers over required area, $N \geq 1$